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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,941	02/01/2002	Jose P. Pereira	N1-P113	8777

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SHEMWELL GREGORY & COURTNEY LLP  
4880 STEVENS CREEK BOULEVARD  
SUITE 201  
SAN JOSE, CA 95129

EXAMINER
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VERBRUGGE, KEVIN

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/061,941

Applicant(s)

PEREIRA ET AL.

Examiner

Kevin Verbrugge

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 February 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-107 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 39-63 and 76-107 is/are allowed.
- 6) ☒ Claim(s) 1-19, 23-38, 64-71 and 73-75 is/are rejected.
- 7) ☒ Claim(s) 20-22 and 72 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4, 7, 10, 11. 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Objections***

Claim 35 apparently erroneously depends on claim 4. Presumably it should depend on claim 34. Correction is required.

Misnumbered claims 45 (second occurrence) through 106 have been renumbered 46 through 107. Additionally, the dependency of each dependent claim from 48 to 107 has been incremented by one to match the new claim numbers created by the renumbering. Since the file copy has already been amended as such, Applicant is required to adopt this change in all future correspondence and claim lists.

Claim 100 (original claim 99) apparently erroneously depends on claim 98 (original 97). Presumably it should depend on 99 (original 98). Correction is required.

### ***Double Patenting***

Claims 1-107 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-129 of copending Application No. 10/062307. Although the conflicting claims are not identical, they are not patentably distinct from each other because the differences are immaterial.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9, 11, 12, 17, 18, 19, 29, 31, 36, 73, 2, 23, 32, 65, 3, 24, 33, 66, 70, 71, 4, 7, 8, 25, 28, 34, 67, 5, 6, 13, 14, 15, 16, 26, 27, 35, 37, 38, 68, 69, 74, 75 and 64 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,526,604 to Hsu et al., hereinafter simply Hsu.

Hsu discloses a variable page size translation lookaside buffer (TLB) relevant to the instant invention. First of all, it should be noted that Hsu teaches that the general method of accessing a TLB is referred to as "hashing". At column 1, line 32 through column 2, line 4, he discloses that there are three types of TLBs: direct-mapped, set associative, and fully associative. The fully associative TLB uses a content addressable memory and can place any address in any location. But the direct-mapped and set associative TLBs are restricted in where they can place addresses and he explains this restriction at column 1, lines 35-65. Basically each address has only a single line of the

TLB where it may be stored, and this line is determined by the index bits of the address which are chosen by a hashing function.

These index bits are shown, for example, in Figs. 3A-3G as index bit field 304, having 7 bits in the figures. The number of index bits is determined by the size of the TLB (7 bits for a TLB with  $2^7$  lines, see column 3, lines 54-60) and the index bits are retrieved from the virtual address by a hashing function (see column 1, lines 37-39 where Hsu teaches that “a subset of bits [index] of each virtual address is used to hash the virtual address to a TLB entry”, emphasis added). In this clear teaching, hashing is simply using certain bits of a virtual address to obtain an index into the TLB, hence these bits are typically referred to as “index” bits. By definition, hashing is converting a key (virtual address in this case) into a value (index) for the location of the corresponding data in a structure (TLB). This is the first meaning of the word “hashing” as used by Hsu. Even though the index bits are simply extracted from the virtual address, it can be said that the entire virtual address is hashed to produce the index bits.

A second use of the word hashing is shown by Hsu in Fig. 4, where hashing circuit 404 is used to combine 7 chosen index bits with 7 ASID bits using an exclusive OR function which then outputs 7 bits which are used as an index into the TLB.

In both cases then, the result of the hashing is the production of an index into the TLB which selects a row of the TLB to activate.

Regarding claims 1, 9, 11, 12, 17, 18, 19, 29, 31, 36, and 73, Hsu shows the step of generating an index (output from XOR circuit 404) based on a search value (virtual address) in Fig. 4. He discusses the step of determining whether the search value matches a data value stored at a memory location indicated by the index at column 7, lines 7-10.

Finally, although he does not explicitly show it or discuss it, his device inherently outputs the index from the high portion of RAM 104 to the low portion of RAM 104. This is a required operation since "the high portion and low portion of RAM 104 are implemented in physically separate memories" (column 4, lines 4-6). The high portion stores virtual addresses (see Fig. 2A for an exemplary entry) and the low portion stores physical addresses (see Fig. 2B for an exemplary entry). The index is output by the high portion of RAM 104 so that the corresponding low portion of RAM 104 will be activated. This is the typical operation of TLBs, CAMs, and caches in general, as disclosed by Applicant in the specification at paragraph 0002, third sentence, where it is admitted "If the search value matches an entry, the CAM device generates an index that corresponds to the location of the matching entry within the storage array, and asserts a match flag to signal the match."

Hsu discusses what his device does when a match occurs at column 6, lines 15-18 and column 7, lines 10-12. Basically if a stored virtual address in the high portion of RAM 104 matches the search virtual address, the index of the matching stored virtual address is applied to the corresponding data storage section in the low portion of RAM 104 and the physical address stored therein is output, indicating a match.

An indication of whether the search value matches the data value is output by page address output circuit 112 on line 160 as taught at column 6, lines 15-18.

Regarding claims 2, 23, 32, and 65, Hsu's device selects a portion of the virtual address and generates the index based on the selected portion, as shown in Fig. 4.

Regarding claims 3, 24, 33, 66, 70, and 71, Hsu's device selects the portion of the virtual address based on a configuration value determining the page size in question as shown in Fig. 4. Different page sizes will cause different virtual address bits to be selected by mux 400.

Regarding claims 4, 7, 8, 25, 28, 34, and 67, Hsu shows the claimed assembling of dispersed fields within a search value to create a search key in Fig. 1 where he shows that virtual address bits 63:62 and 47:19 are input to page address output circuit 112. This is discussed at column 4, lines 1-44.

Regarding claims 5, 6, 13, 14, 15, 16, 26, 27, 35, 37, 38, 68, 69, 74, and 75, Hsu shows the claimed masking at Figs. 5, 6, and 7.

Regarding claim 64, Hsu shows the claimed plurality of indices as the seven 7-bit indices at the top of Fig. 4 being input to mux 400, which selects one of them according to the page size 140 select value, as claimed. Then Hsu's device determines whether

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the search value matches a data value stored in the memory location indicated directly by the selected index (in the case of global input 144 being asserted which deactivates the hashing means 404 and passes the 7-bit index from mux 400 to output 128) or indirectly by the selected index (in the case of global input 144 being not asserted which activates the hashing means 404 and hashes the 7-bit index from mux 400 with the 7-bit ASID value to create a new index which is sent to output 128).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,526,604 to Hsu et al., hereinafter simply Hsu.

Hsu does not disclose using the claimed CRC method for generating his hash value, rather he discloses using XOR. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use CRC for its attendant advantages since it was another well-known hashing algorithm at the time of the invention.



***Allowable Subject Matter***

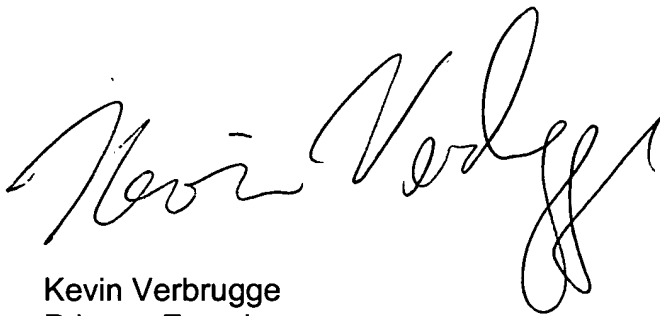
Claims 20, 21, 22, and 72 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 39-63 and 76-107 are allowed.

***Conclusion***

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (703) 308-6663.

Any response to this action should be labeled appropriately (serial number, Art Unit 2188, and After-Final, Official, or Draft) and mailed to Commissioner for Patents, Washington, D.C. 20231, faxed to (703) 872-9306, or delivered to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor Receptionist.

A handwritten signature in black ink, appearing to read 'Kevin Verbrugge', with a stylized, cursive script.

Kevin Verbrugge  
Primary Examiner  
1/23/04